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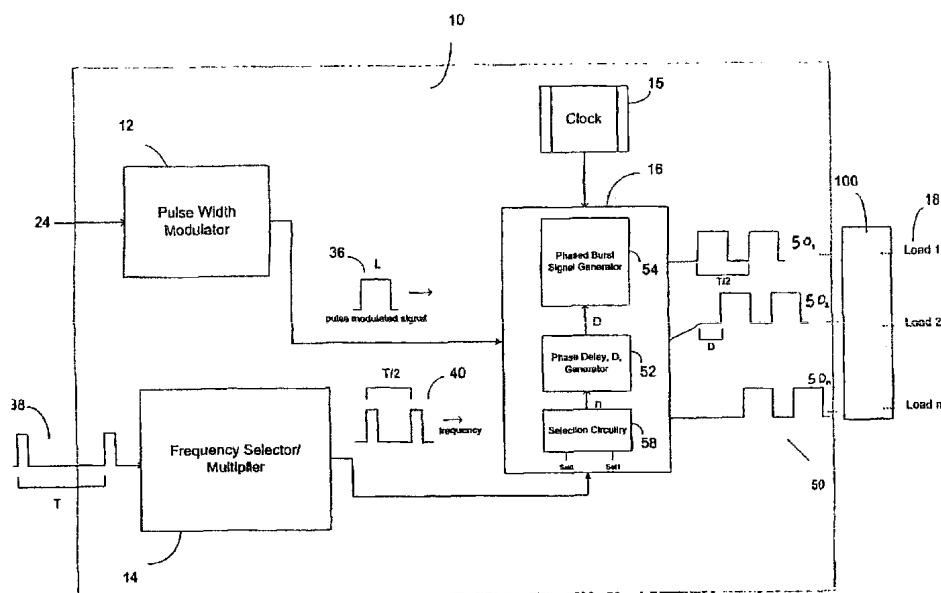
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(54) Title: SEQUENTIAL BURST MODE ACTIVATION CIRCUIT



(57) Abstract: A sequential burst mode regulation system to deliver power to a plurality of loads. In the exemplary embodiments, the system (10) of the present invention generates a plurality of phased pulse width modulated signals (36) from a single pulse width modulated signal, where each of the phased signals regulates power to a respective load. Exemplary circuitry includes a PWM signal generator, and a phase delay array that receives a PWM signal (12) and generates a plurality of phases PWM signals which are used to regulate power to respective loads. A frequency selector circuit (14) can be provided that sets the frequency of the PWM signal (36) using a fixed or variable frequency reference signal.

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SEQUENTIAL BURST MODE ACTIVATION CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a sequential burst mode activation circuit. More particularly, the present invention provides a circuit topology for improving the consistency of performance in the activation and intensity variation of multiple loads. The present invention has general utility wherever multiple loads are employed for intensity variation. Further, the present invention has specific utility where multiple fluorescent lamps, especially multiple cold cathode fluorescent lamps (CCFLs), are employed, for example, in television and computer screens, and in backlights for LCDs (Liquid Crystal Displays).

2. Description of Related Art

Various lighting and dimming circuits and techniques for lighting or dimming lamps or varying intensities of loads are known. One method of dimming a fluorescent lamp, especially as used in a backlight of a liquid crystal display (LCD), is known as a voltage controlled dimming system. The voltage controlled dimming system includes current control and current feedback control. According to the voltage control dimming system, dimming is performed by varying an input voltage to an inverter so as to adjust an output voltage from the inverter (i.e., an application voltage to the fluorescent tube). As the fluorescent tube emits light using discharging energy, when the application voltage to the fluorescent tube is too low, the discharging becomes unstable. For this reason, a large dimming range cannot be achieved by the voltage control dimming system, and the possible dimming ratio is only around 2:1, the dimming ratio being indicative of the dimming range of the lamp system.

Another technique for dimming a fluorescent lamp is the "burst mode" dimming system in which an alternating signal that is supplying power to the lamp is cut with a notch of variable width so as to reduce the power applied to the lamp and thereby provide the desired dimming. The smaller the widths of AC power provided to the lamp, the lower the luminance at which the lamp operates. A common device for providing the ability to vary the width of the pulses are commercially-available pulse-width modulators ("PWM").

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1 In burst mode dimming, dimming is performed by periodically flashing the
2 light source with a varying time ratio between the light-on duration and light-out
3 duration. Therefore, this system, as opposed to the aforementioned voltage controlled
4 dimming method, offers a large dimming ratio, potentially greater than 100:1, thereby
5 allowing for large variations in luminosity.

6 U.S. Patent No. 5,844,540 provides lighting/dimming circuitry for the back
7 light control function in an LCD (Liquid Crystal Display). A "PWM dimmer driving
8 circuit" modulates the magnitude of current to be supplied through an inverter to a
9 fluorescent tube on the back surface of a liquid crystal panel. One goal of this
10 circuitry is to prevent inconsistency of lighting, or occurrence of flicker, between the
11 back light, or fluorescent tube, and the LCD; the other goal is to reduce sound noise.
12 The PWM and inverter circuitry modulates the light source driving means so as to
13 have the ability to periodically flash the light source with varying time ratios between
14 the light on and light off durations, thereby creating different average intensities of
15 light. The light-on duration is determined by a 'pulse count circuit' which provides
16 an input for the PWM circuitry; this pulse count circuit counts the number of pulses of
17 the LCD panel horizontal synchronizing signal, and provides for an on-duration that
18 allows for the back light to synchronize its lighting signal with that of the LCD.
19 Further, the lighting/on-off frequency of the light source is a division of the horizontal
20 driving frequency of the LCD panel's horizontal synchronizing signal, thereby
21 allowing both LCD panel's display and the back light to be in phase with each other.
22 This topology provides a "burst-mode" dimming system but only for a single
23 fluorescent lamp. It further advocates synchronization of backlight lighting with that
24 of the LCD in order to prevent inconsistency of lighting between the LCD and
25 backlight. Note that fluorescent lamps, especially cold cathode fluorescent lamps, are
26 high in impedance when initially powered up. If multiple CCFLs (cold cathode
27 fluorescent lamps) were utilized, synchronization of all lamps with one light source
28 would result in current ripples; these current ripples retard inverter performance and
29 cause flicker. This is because, where multiple CCFLs are synchronized, a power
30 supply needs to provide enough power to turn on all CCFLs concurrently. The instant
31 power delivered from the power supply causes the supply voltage to drop due to its
32 limited dynamic response. Therefore, the use of PWM signals, i.e. "burst-mode"

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1 dimming, is not, by itself, effective in providing a solution to flicker/noise in multiple
2 lamp configurations.

3 One technique used to compensate for flicker or noise in the burst-mode
4 dimming of multiple CCFLs is to place a capacitor in series with the power supply to
5 absorb power surges that cause the current ripples. A drawback of this technique is
6 that, when the lamps turn off in each burst mode cycle, the power supply line, which
7 has an intrinsic inductance, continues to carry current which charges the capacitor,
8 yielding an increase in output voltage.

9 Prior art teachings with the activation with multiple loads, where the loads are
10 not fluorescent lamps, do not address the flicker or noise problem presented by the
11 activation of multiple lamps.

12 SUMMARY OF THE INVENTION

13 Accordingly, the present invention solves the drawbacks of the prior art by
14 providing a sequential burst mode activation circuit for multiple loads by generating a
15 phase shift between multiple burst-mode signals. The burst mode signals are used to
16 regulate power delivered to loads, where each load is regulated by a separate phase-
17 shifted burst signal such that at least two loads do not turn on synchronously. The
18 circuit of the present invention overcomes prior art regulation circuits by eliminating
19 instantaneous high current ripples and noise created by multiple loads turning on
20 simultaneously.

21 The present invention provides a sequential burst mode activation circuit
22 comprising a variable power regulator, comprising a pulse modulator generating a
23 pulse signal having a pulse width; a frequency selector generating a frequency
24 selection signal; and a phase delay array receiving said pulse signal and said
25 frequency selection signal, and generating a plurality of phased burst signals, wherein
26 at least two of said phased burst signals have different start times.

27 In method form, the present invention provides a method for generating phase
28 shifted burst mode signals, comprising the steps of generating a pulse signal having a
29 pulse width, generating a frequency selection signal, generating a plurality of phased
30 burst signals having a frequency of said frequency selection signal and pulse width of
31 said pulse signal, and delaying at least one of the phased burst signals to have a
32 different start time than at least one other of the phased burst signals.

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1 The present invention also provides a phased burst mode dimming system,
2 comprising: a pulse width modulator generating a pulse width modulated signal; a
3 variable selector for selecting the width of said pulse width modulated signal; and a
4 phase delay array receiving said pulse modulated signal and said frequency selection
5 signal, and generating a plurality of phased burst signals by generating a phase delay
6 between at least two said pulse width modulated signals.

7 In one exemplary embodiment, power is regulated to a plurality of loads using
8 the plurality of phased burst signals. Additionally, a constant or variable phase delays
9 is generated between each phased burst mode signal. In an exemplary system, the
10 present invention provides a sequential burst mode dimming circuit for multiple
11 lamps. In particular, the exemplary system provides a sequential burst mode dimming
12 circuit for a plurality of cold cathode fluorescent lamps (CCFLs). Customer or
13 software inputs vary the pulse width of a PWM signal, thereby determining the power
14 to be delivered to the lamps. A reference signal is doubled to select the frequency of
15 the PWM signal. This selected frequency determines the frequency at which lamps
16 turn on and off. Using a counter and a clock, multiple phased burst signals are
17 generated from the above burst signal for the plurality of CCFL's. Each phased burst
18 signal is shifted by a constant phase shift such that at least two lamps receive burst
19 signals that are out of phase. Therefore, sequential burst-mode activation of each lamp
20 is generated. Finally, in the exemplary system, a plurality of phase array drivers, each
21 of which uses feedback from a corresponding lamp in combination with a
22 corresponding phased burst signal, delivers power to and regulates the intensities of a
23 corresponding plurality of lamps.

24 Another exemplary system of the present invention includes a frequency
25 selector that generates a frequency selection signal for a backlight load which follows,
26 as reference, a conventional screen updating frequency of a cathode ray tube (CRT) in
27 a television set. In yet another exemplary system, a phase delay array generates a
28 plurality of phased burst signals, such that no two phased burst signals have different
29 start times. In an example of such an embodiment, a phase delay array generates a
30 constant or variable phase delay so that each of the phased burst signals is delayed by
31 such a phase delay from another of the phased burst signals.

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1 It will be appreciated by those skilled in the art that although the following
2 Detailed Description will proceed with reference being made to exemplary systems
3 and methods of use, the present invention is not intended to be limited to these
4 exemplary systems and methods of use. Rather, the present invention is of broad
5 scope and is intended to be limited as only set forth in the accompanying claims.

6 Other features and advantages of the present invention will become apparent
7 as the following Detailed Description proceeds, and upon reference to the Drawings,
8 wherein like numerals depict like parts, and wherein:

9 Brief Description of the Drawings

10 Figure 1 is a top-level block diagram of an exemplary sequential burst mode
11 signal generation system of the present invention;

12 Figure 2 is a more detailed block diagram of the exemplary sequential burst
13 mode signal generation system of the present invention;

14 Figure 3 is a signal representation of the pulse width modulator of the
15 exemplary sequential burst mode signal generation system of the present invention;

16 Figure 4 is a signal representation of the phase delay array of the exemplary
17 sequential burst mode signal generation system of the present invention;

18 Figures 5(a) and 5(b) are charts of 'select' signal inputs to circuitry reflecting
19 the resulting number of loads;

20 Figure 6 provides a summary of the signals discussed in Figure 1 through
21 Figure 5;

22 Figure 7 is an exemplary IC implementation of the sequential burst mode
23 generation system of the present invention;

24 Figure 8 is a top level diagram of phase array drivers of the present invention;

25 Figure 9 is a circuit example showing how a phase array driver generates a
26 power regulating signal in the present invention;

27 Figure 9a is a signal diagram of the load current;

28 Figure 10 is a timing diagram showing how a phase array driver generates a
29 power regulating signal in the present invention;

30 Figure 11 is a power regulating signal generated by an exemplary phase array
31 driver of the present invention;

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1 Figure 12 is an exemplary IC implementation of a phase array driver IC in the
2 present invention;

3 Figure 13 is a circuit example showing how a phase array driver generates a
4 voltage clamping signal in an exemplary IC of the present invention;

5 Figure 14(a) and 14(b) provide circuit examples of half-bridge and full-bridge
6 (H-bridge) topologies respectively;

7 Figure 15 provides a signal generation example showing the generation of
8 cross switch signals in a full-bridge topology.

9 Detailed Description of the Exemplary Embodiments

10 The following description will reference a burst mode regulating circuit for a
11 plurality of cold cathode fluorescent lamps (CCFLs). CCFLs are arranged, for
12 example, in large panels for displays. Typically, large CCFL panels each utilize a
13 minimum of 6 lamps, and the present invention will describe a burst mode activation
14 circuit with 6 or more CCFLs. Of course, the present invention is not to be limited by
15 a minimum number of loads, nor is it to be limited to CCFLs or any particular type of
16 loads.

17 Figure 1 is a top-level block diagram of an exemplary sequential burst mode
18 signal generation system 10 of the present invention. As a general overview, the
19 sequential burst mode signal generation system 10 operates to generate phase-shifted
20 burst mode signals 50 and sends these burst mode signals to drivers 100 to provide
21 time-delayed regulation of power to a plurality of loads 18. "Burst mode", as used
22 herein and as is understood in the art, generally means regulation of power to a load
23 using a PWM signal to modulate the power delivered to the load based on the pulse
24 width of the PWM signal. System 10 generally includes modulator 12 generating a
25 pulse modulated signal 36, frequency selector 14 generating a frequency selection
26 signal 40 for setting the frequency of the pulse modulated signal, and phase delay
27 array 16 generating multiple phase-shifted burst signals 50. Advantageously, by
28 independently regulating a plurality of loads 18 with a plurality of phase-shifted burst
29 signals 50, thereby substituting the need for a single high power input with the
30 adequacy of multiple low power inputs, the system 10 of the present invention
31 resolves the aforementioned problems with conventional multiple load power
32 regulation circuit.

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1 Figure 2 is a more detailed block diagram of the system 10 of the present
2 invention. Pulse modulator 12 generates a PWM (pulse width modulated) signal 36
3 having a pulse width L, whose duty cycle (i.e. pulse width) determines power
4 delivered to a load 18. The frequency selector 14 selects the frequency of the PWM
5 signal 36, based on an independent reference signal 38 of period, T. In an exemplary
6 embodiment, for reasons that will become apparent below, frequency selector 14
7 comprises a multiplier to multiply the frequency of the reference signal 38 (of period,
8 T) by a factor of k, and generate a multiple signal 40 (of period, T/k), where the
9 multiple signal 40 is used to set the frequency of the PWM signal 36. For example,
10 where the system 10 is utilized to regulate multiple CCFLs, a synchronizing signal, or
11 Vsync, may be used as the reference signal 38. In an example where CCFLs are
12 utilized in television, video, or LCD screens, Vsync 38 is an available video signal
13 used to update the on-screen display. The use of Vsync may be desirable since if an
14 arbitrary reference signal is selected independently of screen updating frequency then
15 a "beat" may occur. A "beat" is understood by one skilled in the art to manifest itself
16 in the following manner. A video display is transmitted across a television monitor
17 by a cathode ray tube (CRT). The CRT, upon completing transmission of a display,
18 returns to a starting position and proceeds to transmit the next display. The displays
19 are refreshed at a frequency defined by Vsync. In the duration between the
20 completion of one display transmission and the initiation of the next, no information
21 is broadcast and the television screen is kept dark. If light is introduced in this
22 duration, the transition of the CRT to its starting position may reveal visual lines
23 superposing different displays. This is known in the art as 'beat.' If the frequency of
24 burst mode regulation of lamps were not to follow Vsync frequency, light would be
25 introduced during the aforementioned duration, thereby allowing for beats. Further,
26 the screen updating frequency is multiplied because if a CCFL frequency is equal to
27 and not a multiple of the screen updating frequency, the concurrent intensities of light
28 may result in flicker. Thus, Vsync is a desired reference signal for the above
29 exemplary applications.

30 In the exemplary embodiment where the reference signal 38 is multiplied to
31 generate the multiple signal 40, it should be noted that when period T/k (k is the
32 multiplier of signal 38) of the multiple signal 40 is greater than L of signal 36, that is,

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1 when period T of signal 38 is greater than $k \cdot L$, each burst signal 50 will comprise
2 distinct pulses. If the period T is equal to or less than $k \cdot L$, then each burst signal 50
3 would be a high DC signal (i.e., each burst signal 50 would represent a full power
4 setting). This is discussed further below. In the example in Figure 2, frequency
5 selector 14 doubles the frequency (i.e., $k=2$) of independent reference signal V_{sync}
6 38, thereby generating a frequency selection signal 40 having period of $T/2$. Both
7 signal 36 and 40 are input into phase delay array 16 to generate a plurality of phased
8 burst signals 50, as described below.

9 Phase delay array 16 includes phase-delay generator 52 to determine a phase
10 delay value, D , between successive phased burst signals, $50_1, 50_2, \dots, 50_n$; load
11 selection circuitry to determine the number of loads n ; and circuitry 54 to generate
12 multiple phase-delayed pulse width modulated signals 50_n . Each of these components
13 is described in detail below.

14 Referring briefly to Figures 5(a) and 5(b), depicted are charts of 'select' signal
15 inputs to selection circuitry 58. These inputs are used to quantify the number n of
16 loads 18 coupled to circuit 10 of the present invention. Note that n also quantifies the
17 number of phased burst signals 50. In an exemplary embodiment, selection circuitry
18 58 operates as a state machine to generate an appropriate signal to the phase delay
19 generator 52 based on the binary value of input "select" signals. Figure 5(a)
20 illustrates "select" signal generation of an exemplary embodiment, where a minimum
21 of 6 CCFLs are utilized. This table includes two inputs: Sel0 and Sel1, each
22 generating a binary value indicative of the number of CCFLs. In this table, 6 CCFLs
23 are represented by Sel0=0 and Sel1=0. Further CCFLs (added by increments of two)
24 are defined in this table. The table of Figure 5 (b) generalizes the above example of
25 Figure 5(a) to include less than a minimum of 6 and more than a maximum of 12
26 CCFLs. Generally, more select signal inputs 58 allow for a greater number of loads
27 18 to be utilized, i.e. a larger n . In this example, an additional select input is
28 provided: Sel2, permitting additional loads to be defined. For reasons that will
29 become apparent below, in the example using CCFLs as loads, it is desirable to define
30 an even number of lamps in the circuit. Of course, those skilled in the art will
31 recognize that the tables of Figures 5(a) and 5(b) and the selection circuitry 58 could
32 be adapted to define any number of loads.

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1 Figure 3 provides a signal representation of the pulse width modulator 12.
2 Pulse width modulator 12 generates a pulse width modulated signal 36 whose pulse
3 width, L , is set by variable selector 24. Variable selector 24 is provided to permit
4 variable power (i.e. dimming) to be delivered to the load by changing the pulse width,
5 L , of the PWM signal. Variable selector 24 varies the value of a DC signal 30
6 proportional to a desired dim setting. In an exemplary embodiment, the variable
7 selector 24 comprises a dim selector 26 and a polarity selector 28. The dim selector
8 26 determines the desired dim setting by increasing or decreasing a DC signal 30.
9 The polarity selector 28 is discussed further below. Oscillator 22 generates a
10 triangular waveform 34 of predetermined frequency as an input to the pulse width
11 modulator 12. The DC signal 30 is superimposed upon the triangular waveform 34.
12 In one exemplary embodiment, illustrated in Figure 3, a section, defined by the
13 intersections of the DC voltage 30 with each of the rise, 25a, and fall, 25b, of each
14 triangular wave 34, determines the leading and falling edges of each pulse, and
15 thereby the pulse width, L , of a pulse width modulated signal 36. In this embodiment,
16 a higher value of DC signal 30 generates a smaller pulse width, L and a lower value of
17 DC signal 30 generates a larger pulse width, L . In an alternative embodiment, a
18 section defined by each falling edge, 25b, and the next rising edge, 25c, is used to
19 generate the pulse width, L . In this alternative embodiment, a higher value of DC
20 signal 30 generates a larger pulse width, L , and a lower value of DC signal 30
21 generates a smaller pulse width, L . The polarity selector 28 determines which section
22 of the intersections of the DC signal 30 and triangular waveform 34 is used to
23 generate the pulse width, L . Thereby, the pulse width modulator 12 generates a PWM
24 signal 36 of pulse width, L , determined by the user selection 24.

25 Figure 4 is a detailed block diagram and signal representation of phase delay
26 array 16. Phase delay array 16 determines a phase delay value, D , and generates
27 phased burst signals 50, as a function of L , $T/2$ and the number n . Phase delay array
28 16 receives as inputs a clock signal 15, PWM signal 36 having pulse width L , select
29 signal inputs 58, and a reference signal 40 of doubled frequency, i.e., having a period
30 of $T/2$. Preferably, the value of D is determined such that the phase shift between
31 each phased burst signal 50 is constant, i.e. D is constant. Further, the phase delay D
32 repeats itself between the last phased burst signal and the first, i.e., where there are n

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1 phased burst signals 50, each pulse, p , of phased burst signal n , 50_n , is preferably
2 leading by phase shift, D , from the next pulse, $p+1$, of phased burst signal 1, 50_1 . To
3 accommodate this in the preferred embodiment, phase delay D equals $(T/2)/n$ where T
4 is the period of reference signal 38, $T/2$ is the period of signal 40, n is the number of
5 phased burst signals 50, and the frequency of each phased signal 50 is equal to the
6 frequency of signal 40. Those skilled in the art will recognize that, alternatively, the
7 present invention may include variable phase delays such that the phase delay value is
8 not constant but that some or all of the loads 18 still turn on at different times. Such
9 alternative embodiments are included in the scope of the present invention.

10 In an exemplary embodiment, circuitry 54 includes a counter 56 with a clock
11 input 15 to generate n phased burst signals 50 given the aforementioned inputs.
12 Specifically, a counter 56 may be implemented with a series of toggling flip-flops
13 wherein a clock pulse at a time of t triggers the first pulse of a first phased burst signal
14 50_1 , while a clock pulse at a time of $t+D$ triggers the first pulse, p , of a second phased
15 burst signal 50_2 . Likewise, the clock pulse at a time of $t+2D$ triggers the first pulse of
16 a third phased burst signal 50_3 and a clock pulse at a time of $t+(n-1)*D$ triggers the
17 first pulse of an n th phased burst signal 50_n . Thereupon, the clock pulse at $t+(n)*D$,
18 triggers the second pulse of the first phased burst signal 50_1 . Since the period of each
19 signal is $T/2$ where T is the period of the independent signal 38, it follows that
20 $[(t+nD) - t]$ equals $T/2$. In other words, $n*D$ equals $T/2$, or D equals $(T/2)/n$.

21 Further, each phased burst signal 50 has pulse width, L . To accommodate
22 this, the first pulse of an m th phased burst signal 50_m , where $1 \leq m \leq n$, is generated
23 by sampling the clock signals starting at clock signal, $t + (m-1)D$, for a duration
24 dictated by variable pulse width L . Subsequent phased burst signals 50 follow the
25 same paradigm. Therefore, the first pulse of the first phased burst signal 50 may be
26 generated from clock pulses, $t, t+1, t+2, \dots, t+(L-1)$, such that L clock pulses account
27 compose the pulse width L of each phased burst signal pulse, p . As noted earlier, to
28 generate distinct pulses for each phased burst signal 50, L should be less than $T/2$.
29 That is, if L is not less than $T/2$, each phased burst signal 50 will be a DC signal with
30 no distinguishable pulses.

31 Figure 6 summarizes signals discussed in Figures 1-5 above for an exemplary
32 embodiment. Signal 34 is the triangular waveform generated by the oscillator 22

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1 (Figure 3). DC signal 30 is superimposed onto signal 34, and shifted up or down, i.e.,
2 increased or decreased, to produce a desired dimming. The intersections of signal 34
3 with DC signal 30 determine the rising and falling edge of each pulse of the pulse
4 width modulated signal 36, thereby determining the pulse width, L, of each pulse of
5 the pulse width modulated signal 36. Signal 36 follows the frequency of signal 34.
6 The pulse width, L, of signal 36 is utilized to generate phased burst signals 50 (i.e.,
7 50_1 to 50_n), while the frequency of signal 36 is not. The frequency of phased burst
8 signals 50 is determined by an independent reference signal, Vsync 38, of period T.
9 Vsync 38 is doubled to generate signal 40 of period T/2, i.e., frequency 2/T. The
10 phased burst signals 50 are timed by this frequency, 2/T. The number of phased burst
11 signals 50 is determined by an input as to the number of loads to be utilized. In the
12 example, six (6) loads are utilized. Therefore, six (6) phased burst signals 50 are
13 displayed, where each phased burst signal, for e.g., 50_2 , lags the previous phased burst
14 signal, for e.g., 50_1 , by $(T/2)/6 = T/12$.

15 Figure 7 is an exemplary IC (integrated circuit) implementation 60 of the
16 sequential burst mode signal generation system 10 of the present invention. The IC
17 60 comprises a PWM generator 12, Vsync detector & phase shift detector 13,
18 frequency multiplier 14, and a phase delay array 16. Components 12, 14 and 16 are
19 described above with reference to Figures 1-5. The exemplary IC 60 also includes a
20 clock 15, an oscillator 22 to generate the triangular waveform 34, buffers 19 to
21 amplify the current driving capacity of phased burst signals, and under voltage
22 lockout protection circuitry 2.

23 The PWM generator 12 receives DIM, polarity, LCT, and a clock (100KHz
24 Generator) signal as inputs. The PWM generator 12 generates a PWM signal 36 as
25 discussed above. Further, as described above, the pulse width of the PWM signal
26 generated by generator 12 is selected using the DIM and polarity inputs. LCT of the
27 exemplary IC 60 is the oscillator 22 input generating the aforementioned triangular
28 waveform of predetermined frequency. The clock 15 is used to measure time
29 increments such that the variable pulse width may be counted.

30 The Vsync detector & phase shift detector 13 receives as inputs, Vsync 38,
31 Sel1, Sel0, and a clock 15. Vsync 38 is an independent reference signal as discussed
32 above. The Vsync detector & phase shift detector 13 detects the presence of an

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1 independent reference signal, Vsync 38, and calculates a phase delay value, D, as
2 described above. In the exemplary IC, if Vsync 38 is not detected, detector 13 utilizes
3 the frequency of the oscillator 22 to generate a reference signal 38. When detector 13
4 detects a Vsync signal 38, the detector 13 abandons the oscillator 22 frequency and
5 adopts the Vsync frequency for signal 38. Detector 13 outputs the phase delay value,
6 D, as well the independent reference signal, 38. Signal 38 along with a clock 15 is fed
7 into a frequency doubler 14, wherein the frequency of Vsync is doubled to generate
8 the burst frequency.

9 In the exemplary IC, the inputs of phase delay array 16 include PWM signal
10 36 from PWM generator 12, a burst frequency value from frequency doubler 14 and a
11 clock 15. As described above, the phase delay array 16 utilizes a counter to generate
12 multiple phase delayed burst signals, wherein each phased burst signal operates to
13 regulate power to a load 18. Each phased burst signal is driven through a buffer 19 to
14 amplify its current driving capacity, and then through a respective phase array driver
15 100. This is discussed further below.

16 The protection circuitry 2 is used to sense the voltage level of a power source
17 (Vcc). When Vcc, shown at pin 26 in Figure 6, increases from low to high, the
18 protection circuit 2 resets the entire IC such that the IC is functionally at an initial
19 status. When Vcc goes low, the protection circuit 2 shuts down the IC to prevent
20 possible damage to the IC.

21 Figure 8 shows a top-level diagram of exemplary phase array drivers 100. In
22 an exemplary configuration, each phase array driver, Driver 1, Driver 2, ... Driver
23 $n/2$, receives two phased burst signals as inputs, and outputs power to two respective
24 loads. The regulation of power to each load is independent of the regulation of power
25 to the other loads. Therefore, alternative configurations allow for each phase array
26 driver 100 to regulate any number of loads totaling more or less than as depicted in
27 the figures. In an exemplary system, each phase array driver 100 receives two phased
28 burst signals 50 which are 180° out of phase and generates two power regulating
29 signals 51 which are 180° out of phase. Phase array drivers 100 translate each
30 variable pulse width L into a duration for which a respective load stays on in each
31 cycle. Therefore, the greater the pulse width of a phased burst signal, the greater the
32 power delivered to the respective load during each cycle. Also each load turns on and

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1 off at the burst frequency defined by the respective phased burst signal 50. Since
2 driver 100 receives complementary signals in the exemplary system, the number of
3 phased burst signals 50 is even for this embodiment.

4 Figure 9 provides an exemplary circuit 200 demonstrating the generation of a
5 load current controlling signal, ICMP, in a phase array driver 100. Figure 10 is an
6 accompanying timing diagram to Figure 9. Figures 9 & 10 are considered together in
7 the following discussion. Also, references are made to Figures 1-5.

8 Circuit 200 comprises an error amplifier 120 generating the current controlling
9 signal, ICMP, a sense resistor R_{sense} 138 coupled in series to a load 18, a switch 134
10 for coupling circuit 200 to the phase delay array 16, and a feedback capacitor CFB
11 139. Additionally, an exemplary circuit 200 includes an RC low-pass filter 136 for
12 filtering noise, and utilizes a transformer 160 to apply the current controlling signal,
13 ICMP, to the load 18. The above components are discussed further below.

14 Generally circuit 200 receives a feedback signal, VIFB, and generates the
15 current controlling signal, ICMP, during two modes of operation. The first mode is
16 soft start and the second mode is burst mode. In soft start mode, the load 18 is
17 powered up from an off state to an operationally on state during a warm up period,
18 utilizing an external soft start controller (not shown). The soft start controller is
19 discussed further below. In burst mode, the duty cycle of the aforementioned phased
20 burst signal 50 (PWM) is utilized to regulate load current, I_L , during the operationally
21 on state of the load 18. That is, in an exemplary embodiment, I_L will be proportional
22 to $[L/(T/K)] \cdot I_{Lmax}$, where L is the pulse width of signal 50, T/k is the period of
23 signal 50, and I_{Lmax} is the load current when the load is fully powered on. In this
24 manner, a load 18 is dimmed during burst mode. This is discussed further below.
25 Note that soft start mode sequentially precedes burst mode. The current controlling
26 signal, ICMP, regulates load current, I_L , during burst mode, but not during soft start.
27 During soft start, ICMP is monitored to determine when to toggle modes from soft
28 start to burst mode. This is explained further below.

29 In both modes, the error amplifier 120 compares the feedback signal, VIFB,
30 with a reference signal, ADJ, and generates the controlling signal, ICMP. In an
31 exemplary embodiment, error amplifier 120 is a negative feedback operational
32 amplifier. ADJ is a predetermined constant reference voltage representing the

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1 operational current of the load 18. This is discussed further below. ICMP varies to
 2 increase or decrease VIFB to equal ADJ. That is, if VIFB is less than ADJ, then the
 3 error amplifier 120 increases ICMP. Conversely, if VIFB is greater than ADJ, then
 4 the error amplifier 120 decreases ICMP. If VIFB=ADJ, ICMP is a constant to
 5 maintain VIFB at ADJ. The operations of exemplary circuit 200 during soft start
 6 mode and during burst mode are discussed in that order and in greater detail below.

7 As stated above, in soft start mode, the load 18 is powered up from an off state
 8 to an operationally on state. Circuit 200 generates the controlling signal, ICMP, based
 9 on the load current, IL, but not based on the respective phased burst signal, PWM 50.
 10 That is, during soft start, circuit 200 is decoupled from phase delay array 16 by switch
 11 134. This is discussed further below. The following discussion proceeds with
 12 reference to ILrms and ILrms (spec). ILrms refers to the root mean square of the load
 13 current, IL at any given moment. ILrms (spec), as used herein, is the manufacturer's
 14 load specifications when the load 18 is operating at full power.

15 In soft start mode, the feedback signal, VIFB is a function of load current, IL.
 16 IL is generally a sinusoidal waveform. Following Ohm's Law, VIFB is proportional
 17 to Rsense * IL. VIFB approximately equals 0.45*Rsense*ILrms and is derived as
 18 follows.

$$19 \quad ILrms = \sqrt{\left[\int_{t_1}^{t_1+T_L} (ILpeak * \sin(t))^2 dt \right] / T_L} = ILpeak / \sqrt{2}$$

20 where T_L is the period of the sinusoid, t_1 and t_1+T_L respectively define the start and end
 21 points of one period of the sinusoid, and $ILpeak$ is the peak load current. Diodes 137
 22 filter out the negative portions of IL, thereby generating a waveform, IL(+), an
 23 example of which is illustrated by signal 400 in Figure 9a, which depicts the half-
 24 rectified current waveform delivered to the load. With the phased burst signal, PWM
 25 50, decoupled from circuit 200, VIFB is effectively the voltage across Rsense. That
 26 is,

$$27 \quad VIFB = \left[\int_{t_1}^{t_1+T_L} Rsense * IL(+) dt \right] / T_L$$

$$28 \quad = (ILpeak * Rsense) / \pi$$

29 Since $ILrms = ILpeak / \sqrt{2}$,

$$30 \quad VIFB = (\sqrt{2} / \pi) * ILrms * Rsense \approx 0.45 * ILrms * Rsense$$

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1 The present invention is not to be limited by this method of determining feedback,
2 VIFB. In the exemplary embodiment, in both soft start and burst modes, the constant
3 reference voltage, ADJ, equals $0.45 \cdot I_{Lrms}(spec) \cdot R_{sense}$, where $I_{Lrms}(spec)$ is
4 generally a constant defined by the load's operational specifications as described
5 above. Therefore, when the load 18 is at full power, i.e., on, as per operational
6 specifications, VIFB will equal ADJ. Since the load 18 is turned on from an off state,
7 at the initiation of soft start mode, IL is effectively zero. Consequently, VIFB is
8 effectively zero, i.e. less than ADJ. Therefore, ICMP is high. As IL is increased by
9 the soft start controller (not shown), VIFB increases, thereby reducing the difference
10 between VIFB and ADJ. Consequently, ICMP decreases. When $VIFB=ADJ$, the
11 load 18 is operationally on as described above, and ICMP carries the energy to
12 regulate the load 18 at its operational current. Therefore, the warm up stage defined
13 by the soft start mode concludes when the energy provided by the soft start controller
14 (not shown) has increased to match that provided by ICMP. At this time, the soft start
15 controller (not shown) ceases control, and ICMP regulates load current. Burst mode
16 begins.

17 In burst mode, circuit 200 generates the controlling signal, ICMP, based on
18 both the load current, IL, and PWM signal 50. Therefore, VIFB no longer adheres
19 solely to the equation, $VIFB=(0.45) \cdot R_{sense} \cdot I_{Lrms}$. Instead, the above equation is
20 supplemented by a factor determined by the presence of PWM signal 50.
21 Consequently, in burst mode, ICMP follows the PWM signal 50 and drives the load
22 18. This is described further below.

23 Switch 134 couples circuit 200 to phase delay array 16 during burst mode. In
24 an exemplary system, switch 134 is a PNP transistor 134 with a reference power
25 source, REF, at its source (or emitter) and the respective phased burst mode signal
26 (PWM) 50 at its gate (or base). The reference power of REF may be derived via a
27 voltage divider circuit (not shown) dividing, for example, an exemplary IC source
28 voltage, VCC (not shown). When triggered by PWM 50, switch 134 couples its drain
29 (or collector) to the REF at its source, transmitting a signal, PWM_52, to circuit 200.
30 In the preferred embodiment, the switch 134 is triggered by a low signal at its gate,
31 and therefore, PWM_52 is complimentary to PWM 50. When PWM 50 is high,
32 transistor 134 is off, and PWM_52 is isolated from PNP 134; that is, no burst mode

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1 information is transmitted to circuit 200, and VIFB follows the equation,
2 $0.45 \cdot I_{Lrms} \cdot R_{sense}$, in an exemplary embodiment. When PWM 50 is low, transistor
3 134 is on, and PWM_52 is high. Rlimit 135 translates PWM_52 current into voltage.
4 This voltage is added to VIFB. Rlimit is chosen such that the voltage added into
5 VIFB effects ICMP to vary load current from an operationally on state to an off state.
6 This is discussed further below.

7 The PWM signal 50 is introduced and PWM_52 generated as described above.
8 When PWM 50 goes low, PWM_52 goes high, and therefore, VIFB exceeds ADJ. To
9 decrease VIFB and match VIFB to ADJ, ICMP goes low. Since ICMP drives the load
10 18, the load 18 effectively turns off. One skilled in the art will recognize that the load
11 18 being off does not require current or voltage to the load 18 to be zero; current or
12 voltage may continue to charge the load 18 minimally when it is off. Then, when
13 PWM 50 goes high, PWM_52 is decoupled from the reference voltage, REF. VIFB
14 returns to the equation $VIFB = 0.45 \cdot I_{Lrms} \cdot R_{sense}$ in the exemplary embodiment.
15 Since the load is effectively off, I_{Lrms} approximates zero. ICMP goes high to build
16 VIFB to approximate ADJ. Consequently, load current, IL, goes high, and the load
17 18 turns on. The result, as seen from Figure 10, is that load current, IL, follows the
18 respective phased burst signal, PWM 50. However, that load current IL also lags the
19 respective burst signal, PWM 50.

20 Figure 11 displays oscilloscope signal readouts of PWM_52, ICMP and load
21 current IL during burst mode operation of an exemplary system of the present
22 invention. PWM_52 is timed with the respective phased burst signal, PWM 50; that
23 is, no significant delay exists between high-to-low or low-to-high transitions of PWM
24 50 and the respective low-to-high or high-to-low transitions of PWM_52. Because
25 the error amplifier 120 has finite charge and discharge current, it takes time to charge
26 or discharge CFB 139 when VIFB goes higher or lower than ADJ, respectively.
27 Consequently, as seen in Figure 11, ICMP lags PWM_52. Since ICMP drives the
28 load 18 during burst mode operation, load current, IL, likewise lags PWM_52.

29 Figure 12 provides an exemplary IC implementation 300 of a phase array
30 driver 100. IC 300 comprises a break-before-make circuit 130 with a half-bridge
31 switching topology. This is discussed further below. In alternative IC
32 implementations, switching topologies such as "full bridge," "forward," or "push-

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1 pull," can be used without departing from the scope of the present invention.
2 Continuing references to Figure 9 are included to explain some operational aspects of
3 IC 300. Exemplary IC 300 receives two phased burst signals (PWM signals) 50
4 which are 180 degrees out of phase with each other. Exemplary IC 300 utilizes these
5 phased burst signals 50 to drive two respective loads whose signals are 180 degrees
6 out of phase with each other. Thus, those skilled in the art will recognize duplication
7 of certain components (e.g., selectors 122, 124 and 126) to drive two individual loads.
8 Of course, IC 300 is only an example, and may be readily configured to drive three or
9 more loads (or a single load). At the outset, description will be made to selectors 122,
10 124 and 126 which may be constructed from generic comparator circuitry and/or
11 custom circuitry to accomplish the signal detection, as set forth below.

12 Exemplary IC 300 comprises an error amplifier 121 for voltage sensing, an
13 error amplifier 120 for current sensing, a current or voltage feedback selector 122, a
14 burst mode or soft start selector 124, and a minimum voltage selector 126. Selectors
15 122, 124, and 126 may be of the same structure, comprising 1 comparator and 2
16 transmission gates, and may be implemented with multiplexers.

17 As described above, each error amplifier 120 generates a current controlling
18 signal, ICMP (shown at pin 4 in the exemplary IC 300) by comparing ADJ with
19 feedback, VIFB (shown at pin 3 in the exemplary IC 300), determined by load
20 current, IL, in soft start mode, and by both IL and phased burst signal, PWM 50, in
21 burst mode.

22 Likewise, Figure 13 provides an exemplary circuit 350 showing an error
23 amplifier 121 for generating a voltage controlling signal, VCMP (at pin 5 in the
24 exemplary IC), by comparing a reference voltage (e.g., 2V) with a voltage feedback
25 signal, VFB (at pin 6 in the exemplary IC 300) determined by load voltage. In an
26 exemplary embodiment, when the load is initially powered on, power delivered to the
27 load by the soft start controller (at input 132), heretofore referred to as SST, is low.
28 That is, the load voltage, V_x , on the secondary side of transformer 160 is low.
29 Consequently, VFB is low. Since the difference between VFB and the reference
30 signal (e.g., 2V) is greater than the threshold of comparison, error amplifier 121
31 generates a high VCMP signal. The relationship between VFB and load voltage is
32 discussed further below. As SST increases, VFB increases and approaches the

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1 reference voltage (e.g., 2V), and VCMP decreases. When VFB matches the reference
2 voltage (e.g., 2V), VCMP is chosen instead of SST to drive load voltage, effectively
3 clamping the load voltage at a predetermined value such that VFB matches the
4 reference voltage (e.g., 2V). Circuitry 360 illustrates the relationship between VFB,
5 and the actual load voltage, V_x , provided at the secondary side of the transformer, in
6 the exemplary circuit 350:

$$7 \quad VFB = V_x * C1 / (C1 + C2)$$

8 Therefore, $C1$ and $C2$ are chosen such that VFB, the voltage feedback signal, reflects
9 a desired factor of load voltage, V_x . For example, if $C2 = 1000 * C1$, then, $VFB =$
10 $V_x / 1000$, that is, VFB is a representation of load voltage which is $1/1000^{\text{th}}$ of load
11 voltage, V_x . In this example, if the reference voltage is 2 Volts, then, the load voltage
12 is clamped at 2000 Volts. Further, analogous to half-wave rectifier diodes 137 of
13 Figure 9, diodes 365 generate a half wave rectified voltage signal. R_y and C_y are
14 peak voltage detectors to detect the peak voltage of the rectified waveform.

15 The current or voltage feedback selector 122 (I_or_V Feedback), selects either
16 the voltage controlling signal, VCMP, or current controlling signal, ICMP, as the
17 signal to drive the load during burst mode operation. In an exemplary IC 300,
18 selector 122 chooses VCMP if load voltage exceeds the aforementioned
19 predetermined value while load current is less than the operational current (i.e., $VIFB$
20 $< ADJ$). Otherwise, selector 122 selects ICMP. Selector 122 may utilize alternative
21 comparisons to determine the selection of a controlling signal, for example, selector
22 122 could be configured to compare ADJ and VIFB to determine if the load has
23 reached operational or predetermined full power. The following discussion proceeds
24 with reference to a controlling signal, CMP, which may either be ICMP or VCMP as
25 described above.

26 In the exemplary IC 300, selector 122 is coupled to the burst mode or soft start
27 selector 124 (CMP_OR_SST). Selector 124 of the exemplary IC 300 determines
28 which of the aforementioned two modes of operation apply, i.e., soft start or burst
29 mode, and toggles from soft start to burst mode when appropriate, as follows.
30 Selector 124 compares CMP and SST (the load power controlling energy generated
31 by the soft start controller) to determine which mode applies and to generate a signal,
32 CMPR, which is either the soft start signal, SST, in soft start mode, or the controlling

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1 signal, CMP, in burst mode. Since, as described above, burst mode is triggered once
2 the load 18 has reached an operationally on state, CMPR is SST prior to SST equaling
3 CMP, and CMPR is CMP once SST equals or exceeds CMP. The soft start controller
4 which provides for the soft start signal (SST) is implemented, for example, by using a
5 capacitor (not shown) externally coupled to pin 13, 132, whose charging rate
6 determines the rate at which the load is powered up. In this example, SST voltage
7 equals $I_s/(C*T)$ where I_s is the current supplied by power source 133 and C is the
8 capacitance of the external capacitor (not shown). The capacitance of the external
9 capacitor (not shown) may be varied to vary the rate at which load current, I_L , is
10 increased during soft start mode. Although soft start mode ends and burst mode
11 begins when CMP matches SST, and CMP regulates power to the load during burst
12 mode, SST continues to increase to VCC.

13 Selector 124 is coupled to a minimum voltage selector, CMPR_or_MIN 126,
14 in the exemplary IC 300. The output of selector is herein referred to as RESCOMP.
15 Selector 126 ensures that a predetermined minimum power is delivered to the load,
16 even when the load is in an "off" state. That is, when power delivered to the load is
17 less than a predetermined minimum value, RESCOMP is a minimum voltage, for
18 example, 740mV. If the load voltage is above the predetermined minimum voltage,
19 then RESCOMP is CMPR (i.e., either CMP or SST as described above).

20 Consequently, in burst mode, whenever PWM 50 goes low and the load turns
21 off as described above, a predetermined minimum voltage is maintained across the
22 load. The desirability of maintaining a minimum voltage across the load is explained
23 below with reference to a CCFL (Cold Cathode Fluorescent Lamp) as an exemplary
24 load.

25 A CCFL is of high impedance when off. Thus, a large voltage is needed to
26 initially induce current through the lamp, that is, to turn on the lamp. In the
27 exemplary IC 300, a large voltage is applied to the CCFL, by the secondary side of
28 transformer 160, to turn on the lamp. Once current has been induced through the
29 lamp, the impedance is decreased, and consequently, voltage may be decreased to
30 operational levels. The predetermined minimum power is maintained across the load
31 thereafter to avoid having to repeat the application of a large voltage to turn on the
32 lamp.

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1 When a predetermined minimum voltage is selected by selector 126, ramp 128
2 functions as a pulse width modulator (PWM) and generates a PWM signal with pulse
3 width determinative of power to the load. The functionality of ramp 128 is analogous
4 to that of pulse width modulator 12 discussed in relation to Figure 3. With reference
5 to this analogy, the DC voltage utilized by the ramp 128 for the generation of the
6 PWM signal is the predetermined minimum voltage. The predetermined minimum
7 voltage, in intersection with the triangular signal 34 discussed in relation with Figure
8 3, generates a PWM pulse width that is minimally adequate to maintain a signal.
9 Effectively, ramp 128 utilizes the predetermined minimum voltage supplied by
10 selector 126, to leave the load minimally powered on when the load is off, during
11 each burst cycle. Where the load voltage is in excess of the predetermined minimum,
12 the power signal determined by aforementioned burst signal PWM 50 is utilized.

13 Break-before-make circuit 130 utilizes the appropriate signals described above
14 to turn a transformer 160 on and off. Note that, alternatively, any suitable switch may
15 be used for this purpose. The exemplary IC 300 includes two switches used in a half-
16 bridge topology, i.e., as a general-purpose DC/AC converter, the outputs of the break-
17 before-make circuit 130, NDRI and PDRI, turn on or off an NMOSFET and
18 PMOSFET respectively, thereby switching a transformer 160 to ground or to VCC
19 (power supply) respectively. Significantly, the break-before-make circuit ensures that
20 the NMOSFET and PMOSFET each turn on exclusively as to the other. That is, the
21 NMOSFET and PMOSFET generate a pair of non-overlapped signals. In an
22 alternative embodiment, four switches are used in a full bridge (H-bridge) topology to
23 switch the transformer 160 to ground or to VCC. The switches convert the DC rail
24 voltage (VCC) to an AC signal which is supplied to the primary side of the
25 transformer, as is well known to those skilled in the art.

26 Figures 14(a) and 14(b) are circuit examples of conventional DC/AC converter
27 topologies using half bridge and full bridge switching schemes, respectively. The half
28 bridge topology exemplified by Figure 14(a) is provided in the exemplary IC 300 and
29 described above. An alternative embodiment utilizes a full bridge (H-bridge)
30 topology exemplified by Figure 14(b). The full bridge topology typically utilizes two
31 NMOSFET and PMOSFET pairs generating two pairs of non-overlapped signals.
32 This is described below with reference to Figure 15. The transformer 160 is turned on

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1 or off by alternating the conduction of pairs of crossed switches, A and D (AD), and B
2 and D (BD), respectively. The break-before-make circuit 130 ensures that AD and
3 BC are not on at the same.

4 Figure 15 provides a signal generation example showing the generation of
5 crossed switch signals (i.e., AD and BC signals) in a full-bridge topology of an
6 exemplary embodiment of the present invention. As discussed in reference to Figure
7 3, oscillator 22 generates the triangular signal 34. Signal 34 is inverted to generate
8 signal 34'. RESCOMP is the output of selector 126. That is, RESCOMP is one of
9 ICMP, VCMP, SST, or MIN (e.g., 740mV). Therefore, RESCOMP is variable. A
10 reference signal, CLK, is utilized to independently toggle switches A and B. In an
11 exemplary embodiment, CLK has a 50% duty cycle and follows signal 34. A second
12 reference signal, PS_CLK, is utilized to independently toggle switches C and D. In
13 the exemplary embodiment, PS_CLK is a CLK signal phased by an adjustable delay,
14 D_{clk} . RESCOMP determines D_{clk} . This is discussed as follows. The positive and
15 negative edge of each pulse of PS_CLK are generated by the respective intersection
16 of the rise of signal 34 and RESCOMP and the respective intersection of rise of signal
17 34' and RESCOMP. Therefore, when RESCOMP increases, as, for example, when
18 the respective phased burst signal 50 goes high during burst mode, the phase delay,
19 D_{clk} , between CLK and PS_CLK increases. The on times of switching pairs, AD and
20 BC, are determined by the overlaps of CLK and PS_CLK. Therefore, when D_{clk}
21 increases, the on times of AD and BC increase, thereby causing more power to be
22 delivered to the respective load. Note, however, that the present invention is not
23 limited by any particular driver architecture, and therefore, not limited to half-bridge
24 or full-bridge topologies.

25 Returning to IC 300 of Figure 12, in the exemplary embodiment, where
26 voltage supplied to the transformer 160 exceeds the source voltage to the IC 300, the
27 break-before-make circuit 130 utilizes "High Voltage Level Shifting". "High voltage
28 level shifting" is explained by the following example. VCC is 5 volts. That is,
29 PMOSFET gate control signal levels vary from ground (0 volts) to VCC (5 volts). If
30 15 volts are fed into the transformer 160, the break-before-make circuit 130 provides
31 a DC voltage shift of 10 volts to the PDRI output, thereby allowing for the PMOSFET

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1 gate control signal to reach 15 volts (10 volts via DC high voltage level shifting + 5
2 volts VCC).

3 Exemplary IC 300 further includes protection circuitry 140. In this IC 300,
4 circuitry 140 is an under voltage lock out circuit (UVLO). At the end of soft start
5 mode, if the voltage delivered to the transformer 160 does not decrease, or if load
6 current, IL, does not reach the specified full operational level, circuitry 140 shuts
7 down IC 300. Primarily, circuitry 140 senses load current and shuts down IC 300
8 during burst mode operation if VIFB is lower than ADJ while maximum power is
9 being delivered to the load. Note that when VIFB is lower than ADJ, error amplifier
10 120 increases output power to the load as discussed above. Therefore, circuitry 140
11 shuts down the IC upon the above condition in order to prevent damage to
12 components from excessive power delivery. Also, protection circuitry 140 is disabled
13 during the soft start duration described above.

14 Thus, it is evident that there has been provided a sequential burst mode
15 regulating circuit that satisfies the aims and objectives stated herein. Those skilled in
16 the art will recognize numerous modifications that can be made to the present
17 invention, and all such modifications are deemed within the spirit and scope of the
18 present invention, only as may be limited by the appended claims.

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CLAIMS

- 1
2 1. A variable power regulator, comprising:
3 a pulse modulator generating a pulse signal having a pulse width; and
4 a phase delay array receiving said pulse signal and a frequency selection
5 signal, and generating a plurality of phased burst signals, each having a frequency
6 determined by said frequency selection signal wherein at least two of said phased
7 burst signals have different start times.
- 8 2. A circuit as claimed in claim 1, wherein each said phased burst signal of said
9 plurality of phased burst signals regulates a respective load.
- 10 3. A circuit as claimed in claim 1, wherein said pulse modulator includes a
11 variable selector for selecting said pulse width.
- 12 4. A circuit as claimed in claim 3, wherein said variable selector comprises a
13 dimmer providing a DC signal, and an oscillator generating a triangular waveform,
14 wherein said pulse width being determined by the intersection of said DC signal and
15 said triangular waveform.
- 16 5. A circuit as claimed in claim 4, wherein said dimmer further comprising a dim
17 selector for setting the DC value of said DC signal, and a polarity selector for
18 determining the section, of said intersection of said DC signal and said triangular
19 waveform, to be used for generating the pulse width of said pulse width modulated
20 signal.
- 21 6. A circuit as claimed in claim 1, further comprising a frequency selector
22 receiving a reference signal and generating said frequency selection signal based on
23 said reference signal, wherein said phase delay array receiving said frequency
24 selection signal and setting the frequency of said pulse signal to said frequency
25 selection signal.
- 26 7. A circuit as claimed in claim 1, wherein said phase delay array includes a
27 counter for timing each said phased burst signal of said plurality of phased burst
28 signals such that at least two of said phased burst signals have different start times.
- 29 8. A circuit as claimed in claim 1, wherein each said phased burst signal has a
30 pulse width equal to said pulse width of said pulse signal.
- 31 9. A circuit as claimed in claim 1, wherein said phase delay array includes a
32 phase delay generator for generating at least one phase delay value.

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- 1 10. A circuit as claimed in claim 9, wherein said at least one phase delay value is a
2 constant.
- 3 11. A circuit as claimed in claim 1, wherein said phase delay array includes at
4 least one select signal input for determining the number of said phased burst signals to
5 generate.
- 6 12. A circuit as claimed in claim 1, further comprising at least one phase array
7 driver receiving at least one said phased burst signal and generating at least one
8 respective power regulating signal for at least one respective load, said power
9 regulating signal having a phase value equal to the phase value of said phased burst
10 signal.
- 11 13. A circuit as claimed in claim 12, wherein each phase array driver receives two
12 said phased burst signals which are 180° out of phase and generates two respective
13 power regulating signals which are 180° out of phase.
- 14 14. A circuit as claimed in claim 12, wherein said phase array driver further
15 comprising soft start circuitry generating power to said at least one respective load
16 during a soft start period, wherein a soft start period defining a period wherein said at
17 least one load is powered from an OFF state to an operationally ON state; and
18 wherein once said load is at least at an operationally ON state, power to said load is
19 regulated by said respective phased burst signal during a burst mode period.
- 20 15. A circuit as claimed in claim 12, wherein said phase array driver further
21 comprising at least one comparator for limiting voltage of said at least one load to a
22 predetermined voltage.
- 23 16. A circuit as claimed in claim 14, wherein said phase array driver including at
24 least one error amplifier, receiving a feedback from said load during said soft start
25 period, and further, receiving feedback from said at least one phased burst signal,
26 wherein said error amplifier generates said at least one respective power regulating
27 signal.
- 28 17. A circuit as claimed in claim 12, wherein said phase array driver further
29 comprising at least one current or voltage feedback selector for selecting either to
30 regulate current to said at least one respective load or regulate the voltage of said at
31 least one respective load.

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- 1 18. A circuit as claimed in claim 17, wherein said at least one current or voltage
2 feedback selector comprises a multiplexer.
- 3 19. A circuit as claimed in claim 14, wherein said phase array driver further
4 comprising a selector for selecting either said soft start period or said burst mode
5 period.
- 6 20. A circuit as claimed in claim 19, wherein said selector comprises a
7 multiplexer.
- 8 21. A circuit as claimed in claim 12, wherein said phase array driver further
9 comprising a minimum voltage selector to regulate power to said at least one
10 respective load with a selected current or minimum voltage.
- 11 22. A circuit as claimed in claim 21, wherein said selector comprises a
12 multiplexer.
- 13 23. A circuit as claimed in claim 12, wherein said phase array driver further
14 comprising a ramp circuit to deliver power to said at least one load.
- 15 24. A circuit as claimed in claim 12, wherein said phase array driver further
16 comprising a DC/AC converter circuitry for generating an AC signal for at least one
17 respective load.
- 18 25. A circuit as claimed in claim 24, wherein said converter includes a transformer
19 for delivering a high voltage to said load based on said AC signal.
- 20 26. A circuit as claimed in claim 12, wherein said phase array driver further
21 comprising protection circuitry for under voltage lock out.
- 22 27. A method for generating phase shifted burst mode signals, comprising the
23 steps of:
- 24 generating a pulse signal having a pulse width;
25 generating a frequency selection signal;
26 generating a plurality of phased burst signals having a frequency of said
27 frequency selection signal and said pulse width of said pulse signal; and
28 delaying at least one of said phased pulse signals to have a different start time
29 than at least one other of said phased burst signals.
- 30 28. A method as claimed in claim 27, further comprising the step of:
31 regulating power to a plurality of loads using said plurality of said phased
32 burst signals, respectively.

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- 1 29. A method as claimed in claim 27, further comprising the step of:
2 generating a constant phase delay between each said phased burst mode signal.
- 3 30. A method as claimed in claim 28, wherein said step of generating a constant
4 phase delay between each said phased burst mode signal comprising the step of
5 dividing the period of said frequency selection signal by the number of loads utilized
6 in said plurality of loads to generate a value for said constant phase delay.
- 7 31. A phased burst mode dimming system, comprising:
8 a pulse width modulator generating a pulse width modulated signal;
9 a variable selector for selecting the width of said pulse width modulated
10 signal; and
11 a phase delay array receiving said pulse modulated signal and said frequency
12 selection signal, and generating a plurality of phased burst signals by generating a
13 phase delay between at least two said pulse width modulated signals.
- 14 32. A circuit as claimed in claim 31, wherein said variable selector comprises a
15 dimmer providing a DC signal, and an oscillator generating a triangular waveform,
16 wherein said pulse width being determined by the intersection of said DC signal and
17 said triangular waveform.
- 18 33. A circuit as claimed in claim 32, wherein said dimmer further comprising a
19 dim selector for setting the DC value of said DC signal, and a polarity selector for
20 determining the section, of said intersection of said DC signal and said triangular
21 waveform, to be used for generating the pulse width of said pulse width modulated
22 signal.
- 23 34. A circuit as claimed in claim 31, further comprising a frequency selector
24 receiving a reference signal and generating a frequency selection signal, wherein said
25 phase delay array receiving said frequency selection signal and setting the frequency
26 of said pulse signal to said frequency selection signal.
- 27 35. A circuit as claimed in claim 31, wherein said phase delay array includes a
28 counter for timing each said phased burst signal of said plurality of phased burst
29 signals such that at least two of said phased burst signals have different start times.
- 30 36. A circuit as claimed in claim 31, wherein each said phased burst signal has a
31 pulse width equal to said pulse width of said pulse signal.

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- 1 37. A circuit as claimed in claim 31, wherein said phase delay array includes a
2 phase delay generator for generating at least one phase delay value.
- 3 38. A circuit as claimed in claim 37, wherein said at least one phase delay value is
4 a constant.
- 5 39. A circuit as claimed in claim 31, wherein said phase delay array includes at
6 least one select signal input for determining the number of said phased burst signals to
7 generate.
- 8 40. A circuit as claimed in claim 31, further comprising at least one phase array
9 driver receiving at least one said phased burst signal and generating at least one
10 respective power regulating signal for at least one respective load, said power
11 regulating signal having a phase value equal to the phase value of said phased burst
12 signal.
- 13 41. A circuit as claimed in claim 40, wherein each phase array driver receives two
14 said phased burst signals which are 180° out of phase and generates two respective
15 power regulating signals which are 180° out of phase.
- 16 42. A circuit as claimed in claim 40, wherein said phase array driver further
17 comprising soft start circuitry generating power to said at least one respective load
18 during a soft start period, wherein a soft start period defining a period wherein said at
19 least one load is powered from an OFF state to an operationally ON state; and
20 wherein once said load is at least at an operationally ON state, power to said load is
21 regulated by said respective phased burst signal.
- 22 43. A circuit as claimed in claim 40, wherein said phase array driver further
23 comprising a comparator for limiting voltage of said at least one load to a
24 predetermined voltage.
- 25 44. A circuit as claimed in claim 42, wherein said phase array driver further
26 comprising at least one error amplifier, receiving a feedback from said load during
27 said soft start period, and further, receiving feedback from said at least one phased
28 burst signal, wherein said error amplifier generates said at least one respective power
29 regulating signal.
- 30 45. A circuit as claimed in claim 40, wherein said phase array driver further
31 comprising at least one current or voltage feedback selector for selecting either to

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- 1 regulate current to said at least one respective load or regulate the voltage of said at
2 least one respective load.
- 3 46. A circuit as claimed in claim 42, wherein said at least one current or voltage
4 feedback selector comprises a multiplexer.
- 5 47. A circuit as claimed in claim 42, wherein said phase array driver further
6 comprising a selector for selecting either said soft start period or said burst mode
7 period.
- 8 48. A circuit as claimed in claim 42, wherein said at least one burst mode selector
9 comprises a multiplexer.
- 10 49. A circuit as claimed in claim 40, wherein said phase array driver further
11 comprising a minimum voltage selector to regulate power to said at least one
12 respective load with a selected current or minimum voltage.
- 13 50. A circuit as claimed in claim 49, wherein said selector comprises a
14 multiplexer.
- 15 51. A circuit as claimed in claim 40, wherein said phase array driver further
16 comprising a ramp circuit to deliver power to said at least one load.
- 17 52. A circuit as claimed in claim 40, wherein said phase array driver further
18 comprising a DC/AC converter circuit generating an AC signal to supply power to at
19 least one respective load.
- 20 53. A circuit as claimed in claim 52, wherein said converter includes a transformer
21 for delivering high voltage to said load based on said AC signal.
- 22 54. A circuit as claimed in claim 40, wherein said phase array driver further
23 comprising protection circuitry for under voltage lock out.
- 24 55. A circuit as claimed in claim 6, wherein said frequency selector comprises a
25 frequency doubler, doubling the frequency of said reference signal, and generating
26 said frequency selection signal having a period twice that of said reference signal.
- 27 56. A circuit as claimed in claim 34, wherein said frequency selector comprises a
28 frequency doubler, doubling the frequency of said reference signal, and generating
29 said frequency selection signal having a period twice that of said reference signal.

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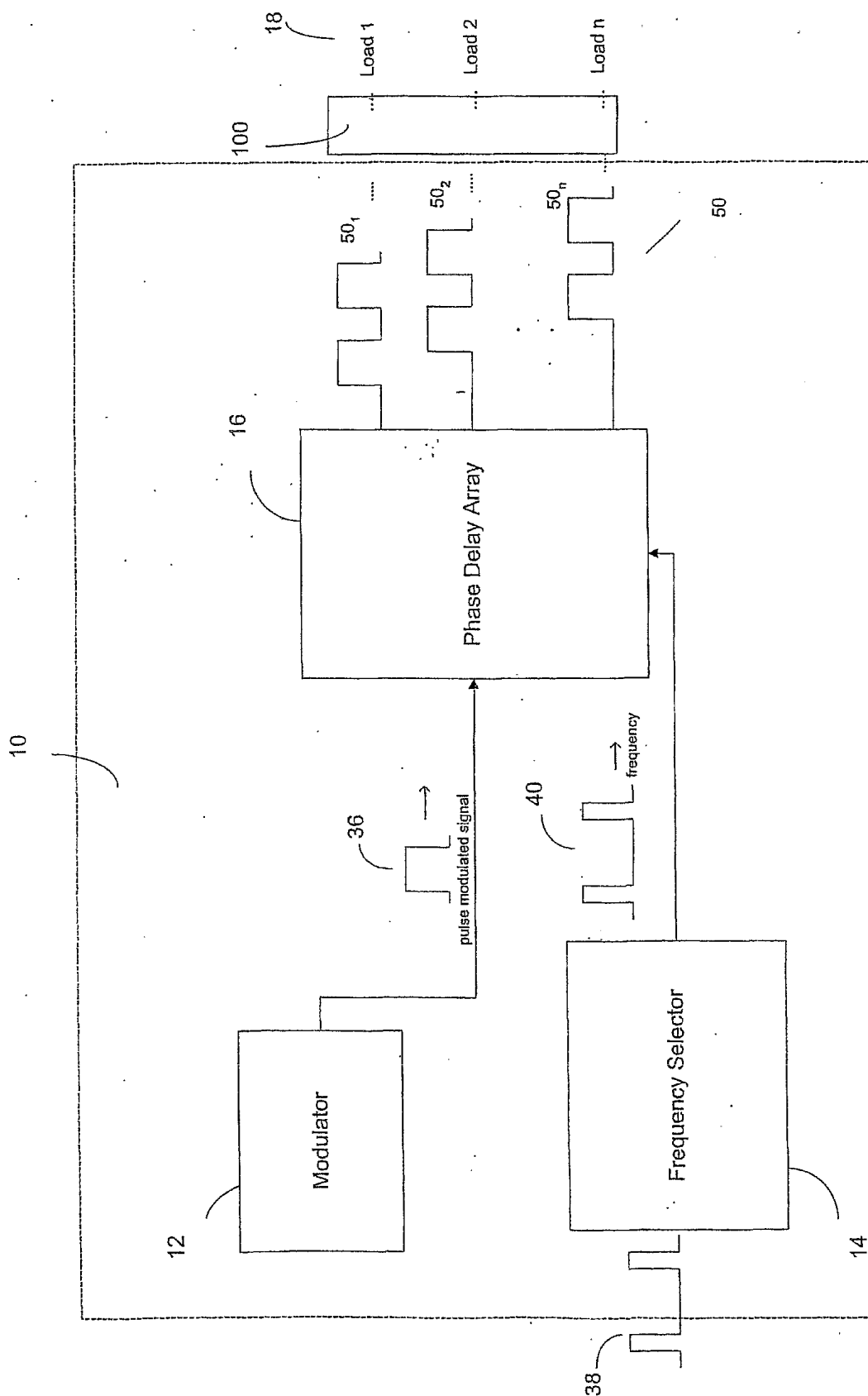
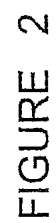


FIGURE 1



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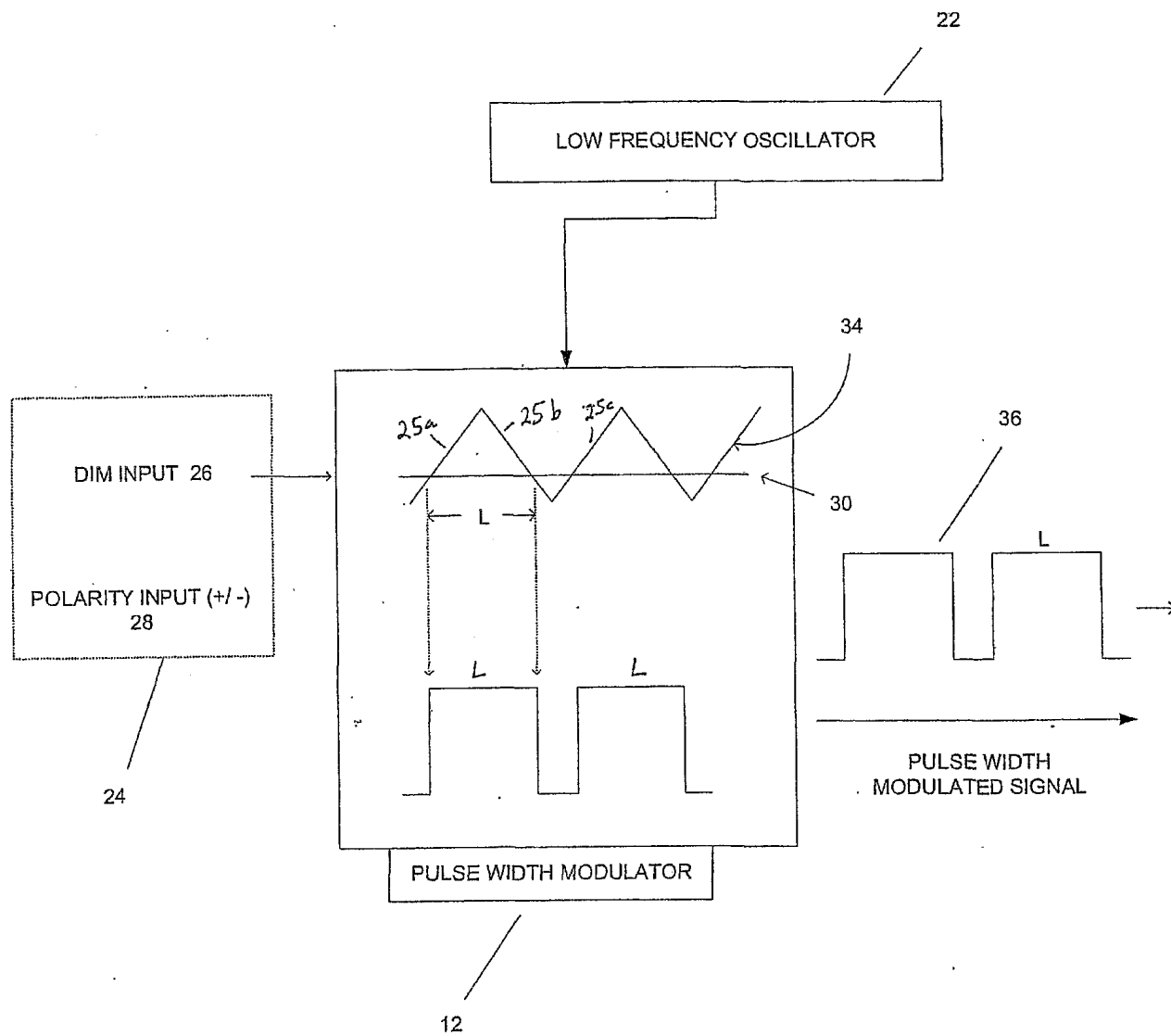


FIGURE 3

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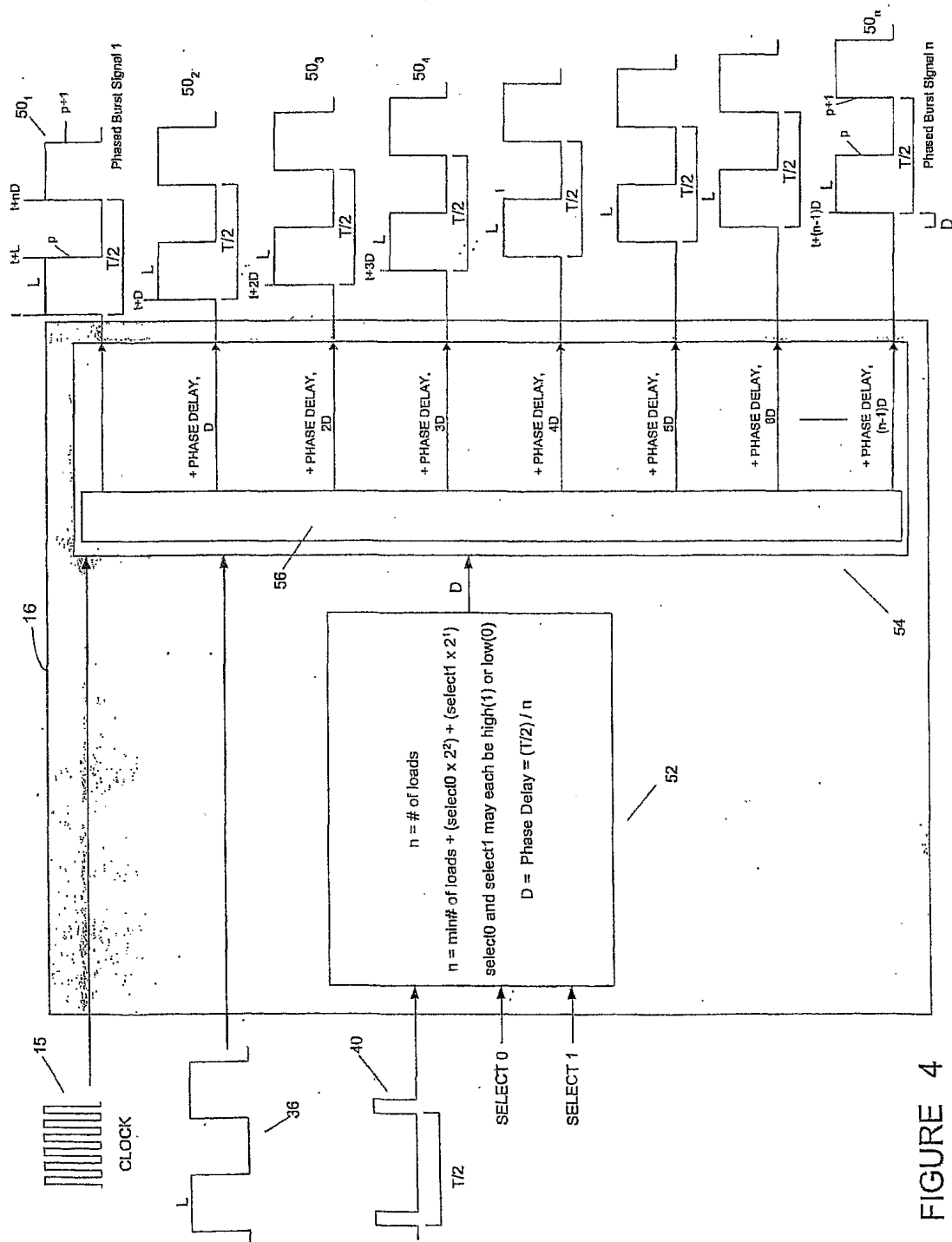


FIGURE 4

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Sel0 (Select 0)	0	0	1	1
Sel1 (Select 1)	0	1	0	1
min# of CCEs	6 (or min#)	8 (min# + 2)	10 (min# + 2)	12 (min# + 2)

FIGURE 5 (a)

Sel0	0	1	0	1	0	1	0	1
Sel1	0	0	1	1	0	0	1	1
Sel2	0	0	0	0	1	1	1	1
min# of Heads	min + 0	min + 2	min + 4	min + 6	min + 8	min + 10	min + 12	min + 14

FIGURE 5 (b)

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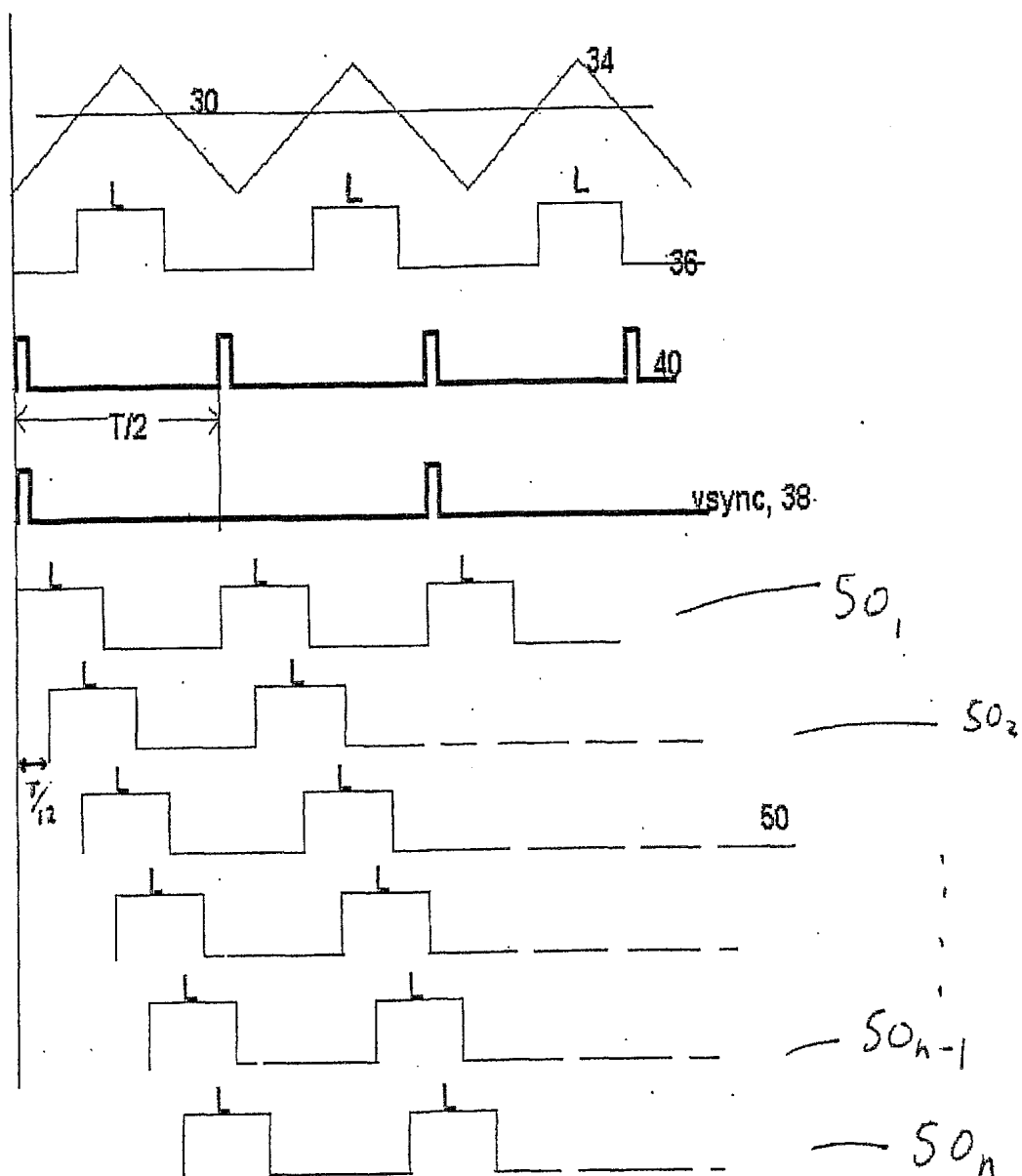


FIGURE 6

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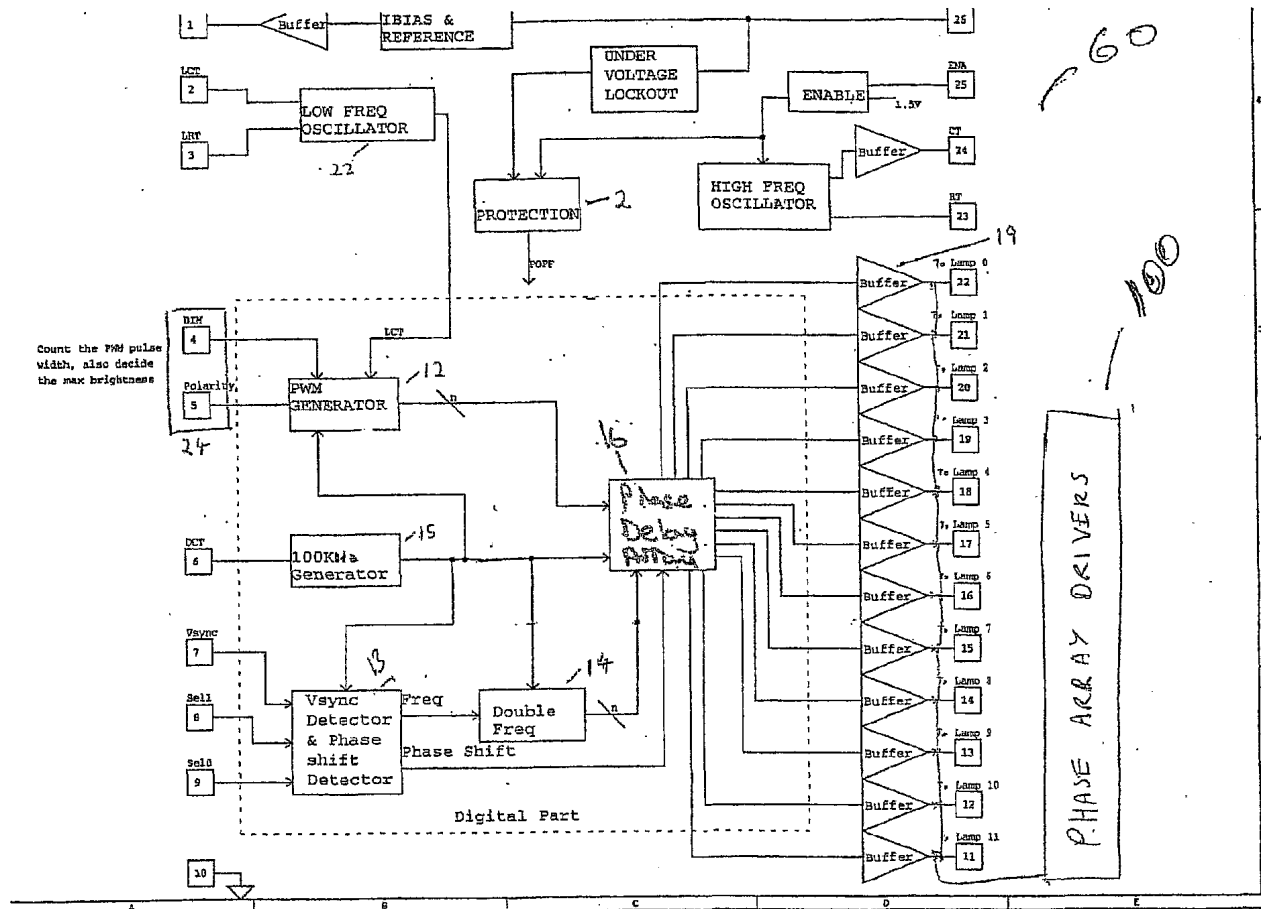


FIGURE 7

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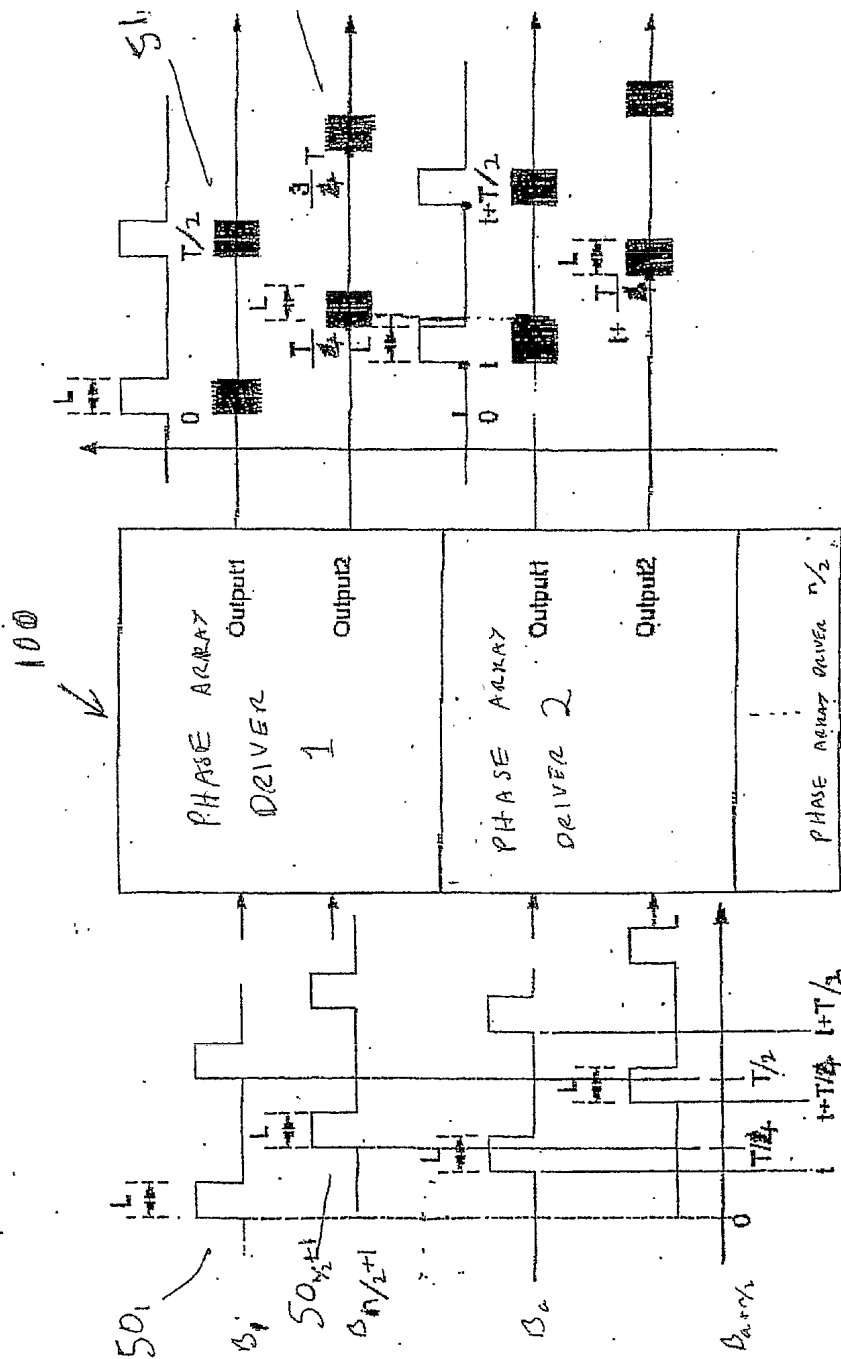


FIGURE 8



FIGURE 9

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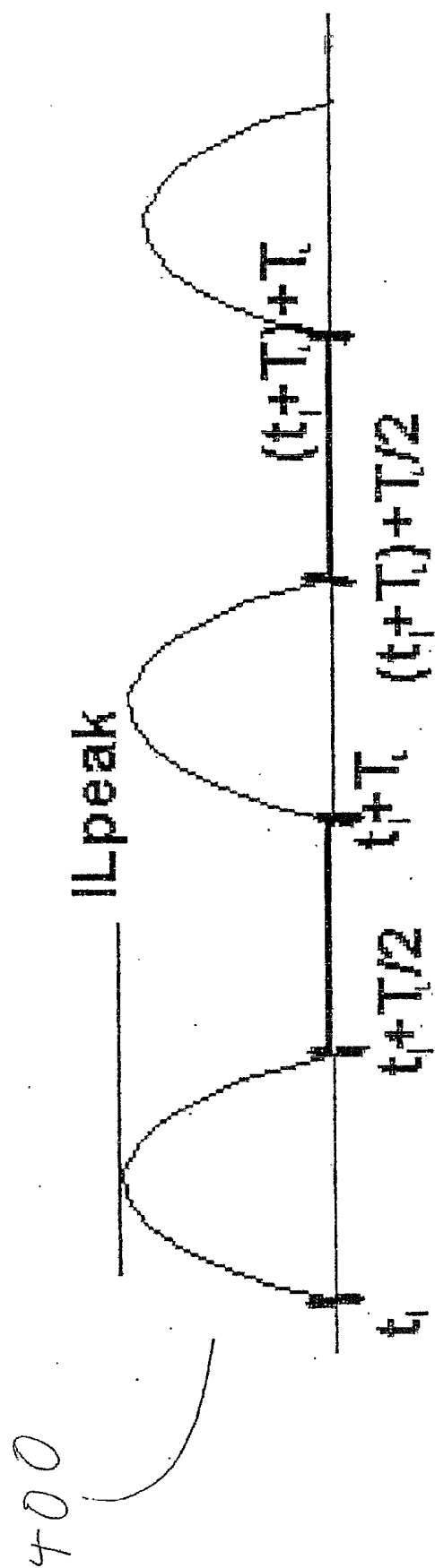


FIGURE 9a

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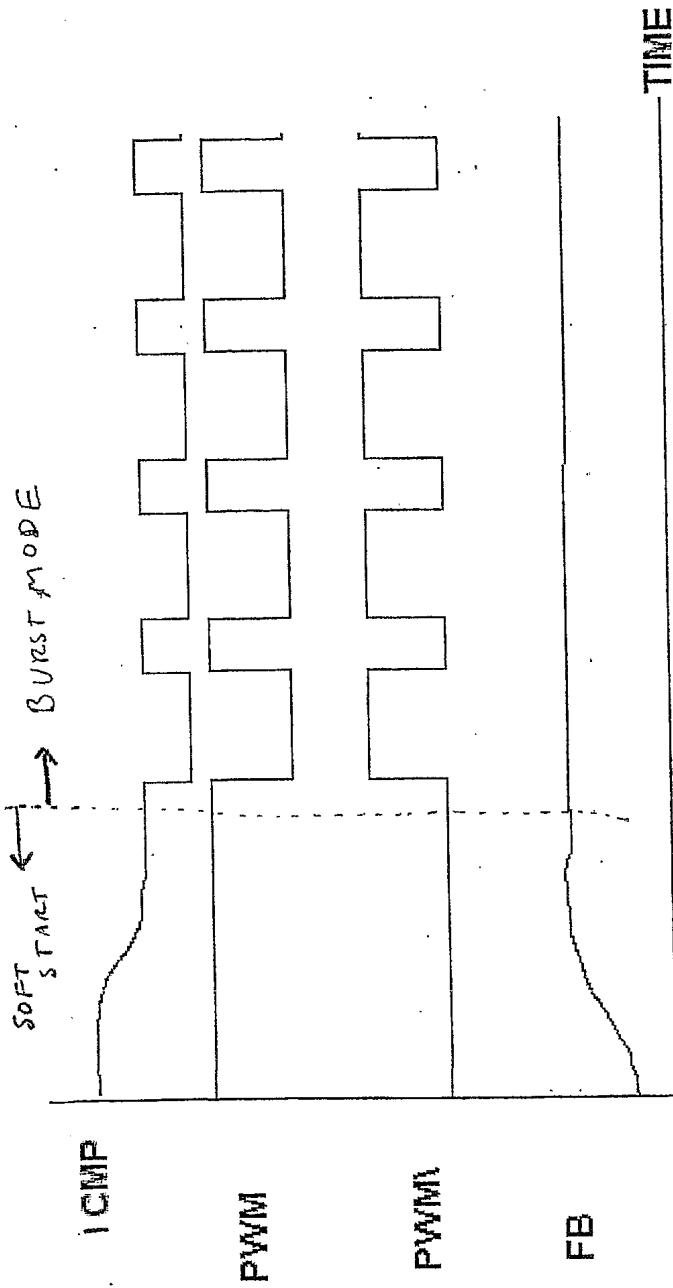


FIGURE 10

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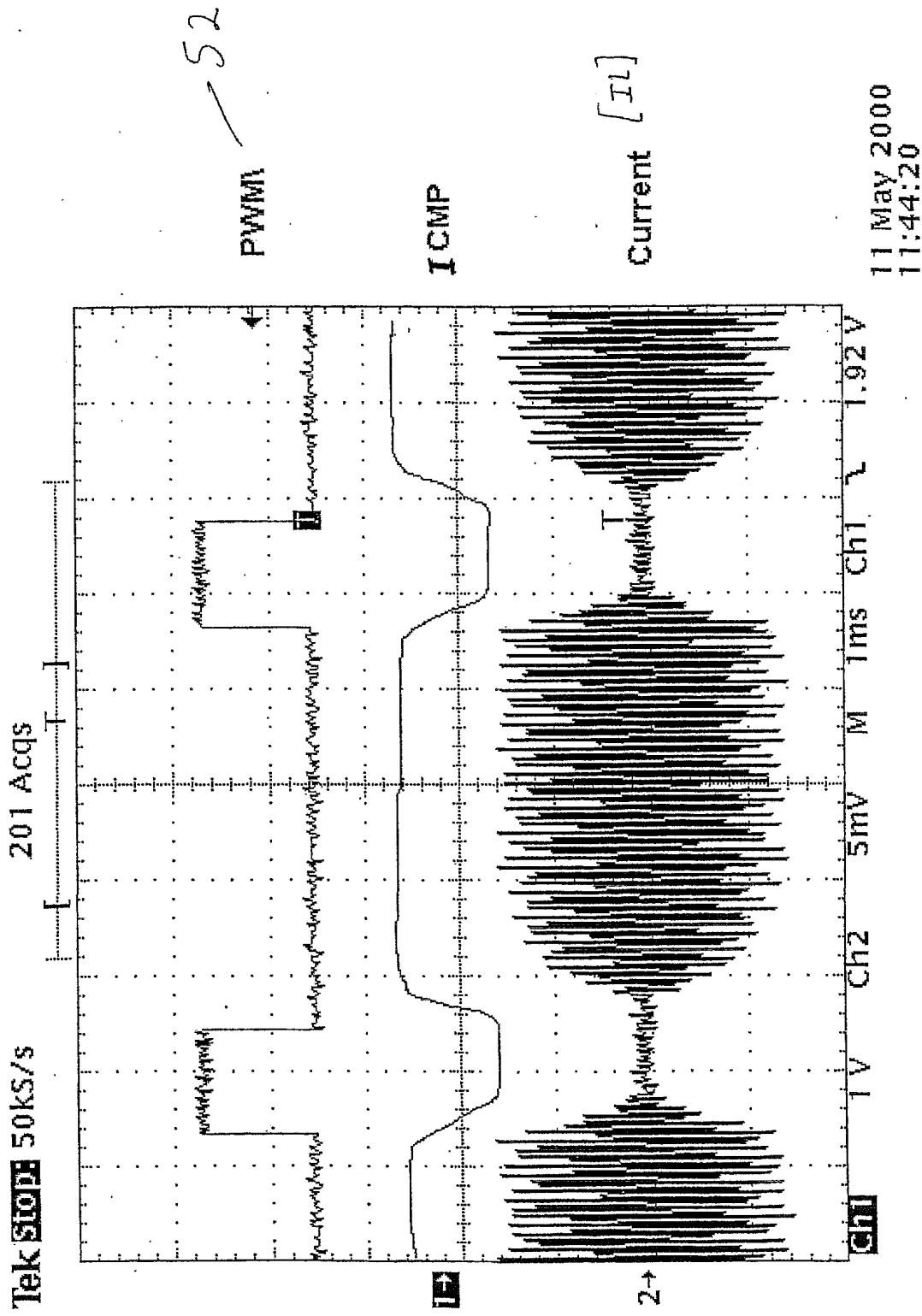


FIGURE 11



FIGURE 12

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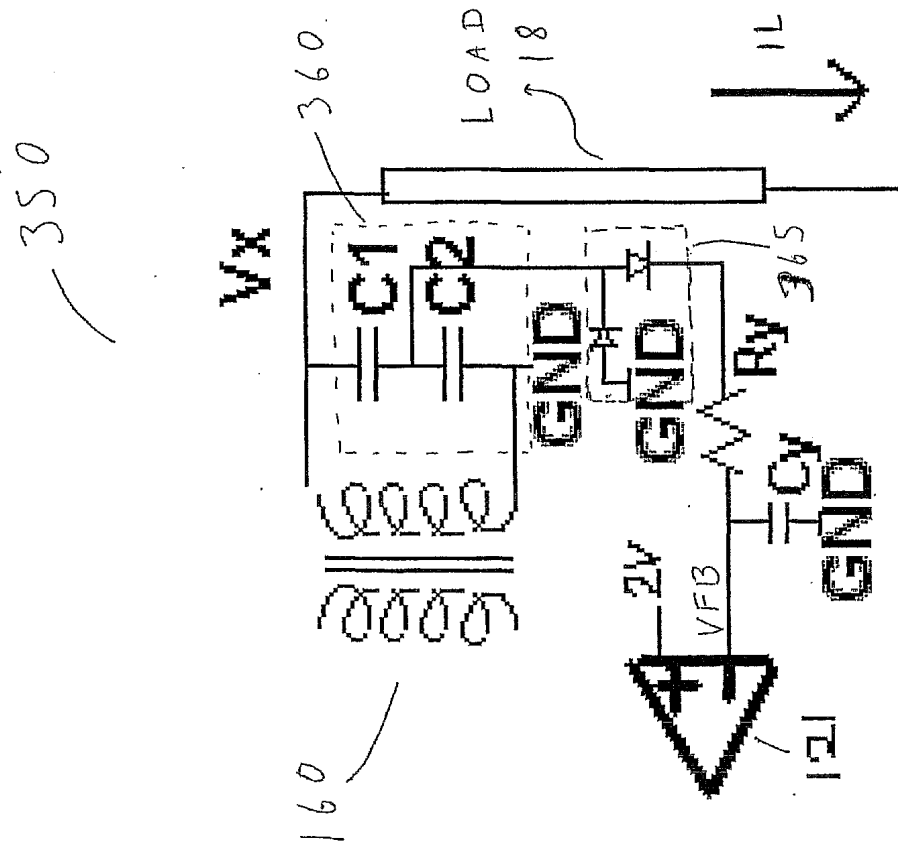


FIGURE 13

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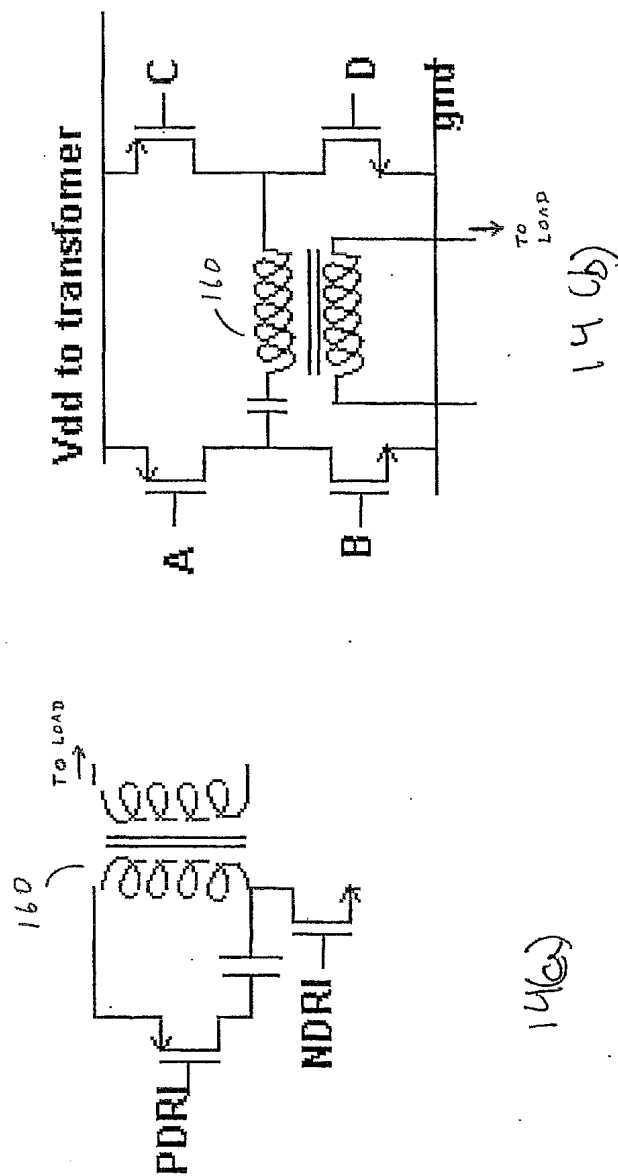


FIGURE 14

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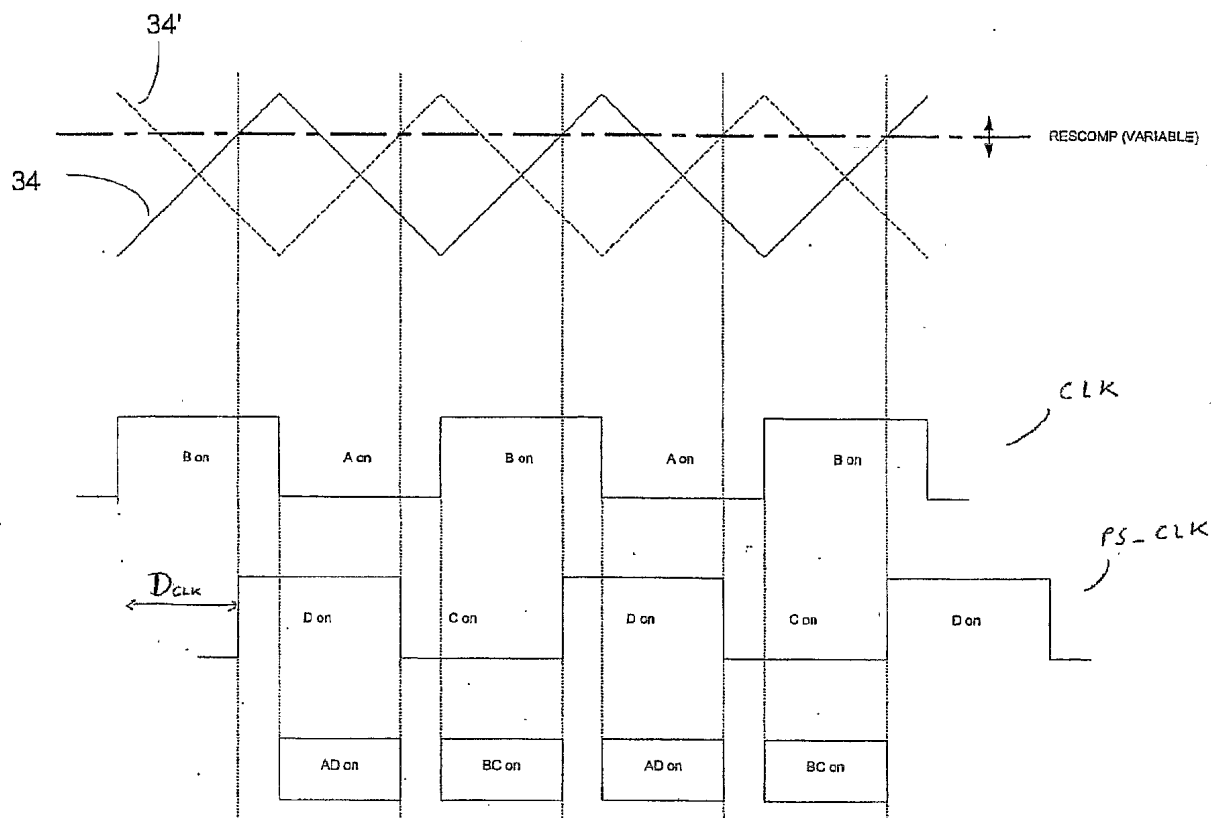


FIGURE 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/00129

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H05B 37/02; H02M 3/335, 3/24

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 315/219, 209R, 224, 225, 291, 307, 308, 226, DIG.5; 363/17, 98, 25, 31, 40, 41, 95, 96, 97

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 6,316,881 B1 (SHANNON et al) 13 November 2001 (13.11.2001), entire document.	1-56
Y,P	US 6,259,615 A (LIN) 10 JULY 2001 (10.07.2001), entire document.	1-56



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
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Date of the actual completion of the international search

08 APRIL 2002

Date of mailing of the international search report

07 MAY 2002

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/00129

A. CLASSIFICATION OF SUBJECT MATTER:

US CL

315/219, 209R, 224, 225, 291, 307, 308, 226, DIG.5; 363/17, 98, 25, 31, 40, 41, 95, 96, 97